A Visual Simulation Tool at Layout Level

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Abstract. *This work presents a Web-based graphical tool that makes it possible to view and simulate a working circuit at the layout level. This tool allows one to observe changes in logical levels with a dynamic alteration of the color properties of the graphical elements that characterize the circuit at layout level. The layout view changes colors in function of logic level changes. Two aspects of the circuit simulation are presented: taking into account the gates delay or not. The Visual System have been entirely developed on JAVA language and it can easily run on any system that supports JAVA, that guarantees the tool a great portability.*

1. Visual Simulation Tool

It is a CAL tool to simulate integrated circuits at layout level with a visual feedback, as well as a simple layout viewer with the most common features (figure 1). The tool does a dynamic visual simulation of integrated circuits at logical level. The user can observe the layout of a circuit at work. This tool provides many visualization modes and allows the user to configure some visualization options, as well as to load your own configuration, that was previously saved. A layout description in CIF format is used as input for the simulator.

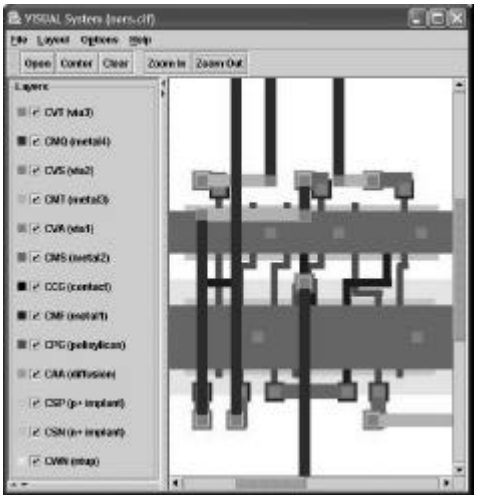

Figure 1 – Visualization of a simple layout

After the interpretation of the input file by the simulator, an internal data structure is built, this data will work as the main data structure for the simulation algorithm. The tool provides a vision that is in some way similar to the view of a circuit that we can have with an electron beam microscopy, based on this the microelectronics teaching can be considerably improved by this tool.

2. Process of Simulation

The algorithm to simulate the circuit uses the main data structure created by the interpretation of the input file. This data structure contains all the necessary information to simulate the circuit, like layout layers,

rectangles that are part of each layer, dimensions, Cartesian coordinates, and logic level of each layout component. Through the layout visualization the user can easily choose a logic value to each input of the circuit and, after that, starts the simulation. With the inputs values of the circuit set by the user, an underground logical simulation is made based on the main data structure, after that, the simulation algorithm constructs a vector of modifications that must be applied on the layout components. So, the user will see a visual simulation of the circuit at work by observing the dynamic change of color properties of the layout components (figure 2) or observe the propagation of the inputs values through the layout. The user can control the speed of propagation of the changes in the circuit input by defining a standard delay of propagation of one change from one block to another. This provides to the user a simulated view of a circuit at work.

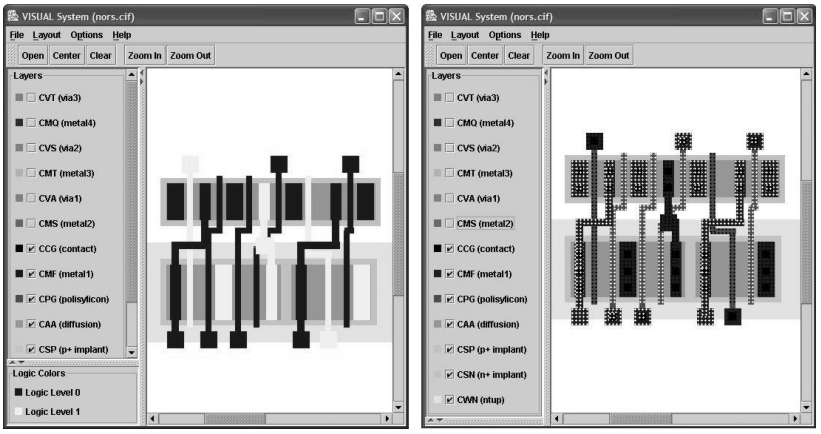

Figure 2 – Visualization of a simulation's result with one color per logic, left, and logic level representation by texture, right.

3. Visualization Modes

The tool provides many visualization modes, as color or gray scale, logic representation through texture, one color per logic level or through a way of colors completely personalized by the user. The tool also has an option to save user's configuration that can be loaded in another section of work. The logic representation through texture maintains the basic color of the layout component and applies a texture according to the logic level of this component. In the logic representation by one color per logic level all the layout components are represented by only two colors, the layout components without an evaluated logic level are shown in the gray scale mode, the user can choose the logic level colors or use the default colors. The tool also provides a mode where the user can completely customize the color representation, choosing for each layer a color to represent each logic level and the basic color for the layer.

4. Conclusions and Future Works

This work presented a brief report on the research and development of a didactic tool to simulate integrated circuits at layout level [CASA 2003]. The Visual System allows visual simulation and visualization of integrated circuits at layout level. Firstly, the Visual System tool will give the purely logic simulation, but the objective is to improve this simulation using timing verification and attaching a layout extractor to the tool. The main advantages offered by this tool are platform independence and the visual feedback that the user have. This tool will be included to an integrated framework for digital systems and microelectronics education. One didactic aim is to catch the student's attention, motivate his/her studies and strengthen his/her learning with the interactive use of several resources that CAL tools can offer. The experience that a student can have with simulation tools using visual outputs helps a lot the learning process. The visual simulation tool at layout level will be distributed at **http://www.inf.ufrgs.br/gme/dsvl**.

5. References

[CASA 2003] Casacurta, Alexandre; Almeida, Marcel Furtado; Reis, Ricardo Augusto da Luz. A Visual Simulation Tool at Layout Level. International Conference on Microelectronic Systems Education – MSE 2003, Anaheim, California, 1 e 2 de junho de 2003.